In The Claims:

Please replace all prior versions of claims by the following:

1-12. (Cancelled)

13. (Original) An integrated circuit adapted to protect a first and a second internal circuits from electro-static discharge (ESD), the first internal circuit coupled between a first high power line and a first low power line, the second internal circuit coupled between a second high power line and a second low power line, the first and the second high power lines being separated from each other, the first and the second low power lines being separated from each other, the integrated circuit comprising:

a first ESD protection circuit, coupled between the first high and the first low power lines;

a second ESD protection circuit, coupled between the second high and the second low power lines;

a third ESD protection circuit, coupled between the first high and the second high power lines, selectively grounding the first or the second high power lines while ESD occurring on the first or the second high power lines, wherein the third ESD protection circuit comprises a first diode string, a first metal-oxide-semiconductor (MOS) transistor and a second diode string, wherein the first diode string and the first MOS transistor are coupled in series; the second diode string are parallel and reverse to the first diode string and the first MOS transistor, and the first diode string and the first MOS transistor

constitute a parasitic silicon-controlled rectifier (SCR) for providing a discharge route while triggered by ESD; and

a fourth ESD protection circuit, coupled between the first low and the second low power lines, selectively grounding the first or the second low power lines while ESD occurring on the first or the second low power lines, wherein the fourth ESD protection circuit comprises third diode string, a second metal-oxide-semiconductor (MOS) transistor and fourth diode string, the third diode string and the second MOS transistor are coupled in series; the fourth diode string are parallel reverse to the third diode string and the second MOS transistor; and the third diode string and the second MOS transistor constitute a parasitic silicon-controlled rectifier (SCR) for providing a discharge route while triggered by ESD.

14. (Original) The integrated circuit of claim 13, wherein the first and second MOS transistors comprise an N-type or a P-type MOS transistor.

15. (Original) The integrated circuit of claim 13, wherein first series and second diode string of the third ESD protection circuit comprise at least one diode, and the third series and fourth diode string of the fourth ESD protection circuit comprise at least one diode.

16. (Original) The integrated circuit of claim 15, wherein numbers of the first series and second diode string depend on a voltage difference between the first high power line and the second high power supply bus.

17. (Original) The integrated circuit of claim 15, wherein numbers of the third series and fourth diode string depend on a voltage difference between the first low power line and the second low power supply bus.

18. (Original) The integrated circuit of claim 13, wherein the third ESD protection circuit further comprises a third MOS transistor, which is coupled to the second diode string in series; the first and third MOS transistors are coupled to the second high and the first high power lines, respectively; the fourth ESD protection circuit further comprises a fourth MOS transistor, which is coupled to the fourth diode string in series; and the second and the fourth MOS transistors are coupled to the second and the first low power lines, respectively.

19. (Previously presented) The integrated circuit of claim 18, wherein the first, second, third and fourth MOS transistors comprise an N-type or a P-type MOS transistor.

20. (Original) The integrated circuit of claim 16, further comprising:

a first input ESD protection circuit, coupled and among the first internal circuit, an input pad of the first internal circuit, the first high power line and the first low power line; and

a second input ESD protection circuit, coupled and among the second internal circuit, an input pad of the second internal circuit, the second high power line and the second low power line.